

Dietary Recommendations for Lightweight Block Ciphers: Power, Energy and Area Analysis of Recently Developed Architectures







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Overview

- Lightweight Devices and Lightweight Cryptography
- Contribution and Architectures
- Evaluation Methodology
- Results and Discussion
- Conclusion and Future Directions





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- RFID-Tags
- Smart Cards
- Wireless Sensors



APPLICATIONS



Electronic passports

Logistics





Road toll-collection





APPLICATIONS - THE SECURITY NEED





- Control on access: Car key systems, etc.
- Enforcing business models: Electronic wallet, etc.
- Counterfeiting: Batteries, etc.
- Privacy protection: Medical sensors, etc.





IMPORTANT METRICS

- Power and energy consumption
 - Active devices with on-chip batteries
 - Battery-less passive devices that rely on limited EM-transmitted power
- Area and complexity
 - Gate count, I/O pin count, storage



- Algorithms with particularly low implementation costs
 - Tailored to fulfill previously mentioned requirements





LIGHTWEIGHT BLOCK CIPHERS

- Early examples:
 - PRESENT, CLEFIA ISO standards
 - KATAN, mCrypton, etc.
- Recently-developed:
 - KLEIN, LED, PRINCE, etc.



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And many more...



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And many more...

Above are the implemented ciphers in this work!



PRESENT

- 64-bit block size, 80/128-bit key size
- Substitution-permutation network
- 4x4-bit S-box
- 31 rounds
- ISO standard!



CLEFIA

- 128-bit block size, 128/192/256-bit key size
- Feistel network
- 18/22/26 rounds
- ISO standard!



KATAN

- 32/48/64-bit block size, 80-bit key size
- LFSR structure
- 254 rounds
- Extremely efficient in hardware



MCRYPTON

- 64-bit block size, 64/96/128-bit key size
- Substitution-permutation network
- Four 4x4-bit S-boxes
- 12 rounds



KIFIN

- 64-bit block size, 64/80/96-bit key size
- Substitution-permutation network
- 4x4-bit S-box
- 12/16/20 rounds





- 64-bit block size, 64/128-bit key size
- Substitution-permutation network
- 4x4-bit S-box (PRESENT S-box)
- 8*4=32 / 12*4=48 rounds



PRINCE

- 64-bit block size, 128-bit key size
- Substitution-permutation network
- 4x4-bit S-box
- 12 rounds



Regular Block Ciphers

AFS

- 128-bit block size, 128/192/256-bit key size
- Substitution-permutation network
- 8x8-bit S-box
- 10/12/14 rounds
- NIST standard!



Regular Block Ciphers

AFS

- 128-bit block size, 128/192/256-bit key size
- Substitution-permutation network
- 8x8-bit S-box
- 10/12/14 rounds
- NIST standard!

Included in analysis for a fair comparison – to a standard cipher!



Regular Block Ciphers

AFS

- 128-bit block size, 128/192/256-bit key size
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6 different architectures (w.r.t. S-box) investigated



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Contribution

- Up to now, dominant comparison metric: Area
 - Measured in Gate Equivalents (GE)!
 - Helpful but does not answer all questions
- Good power and energy consumption prediction important
 - For battery-powered systems
 - For passive systems
- Extending existing studies to an extensive suite of recent lightweight symmetric schemes



All implementations re-implemented from scratch based on the references!

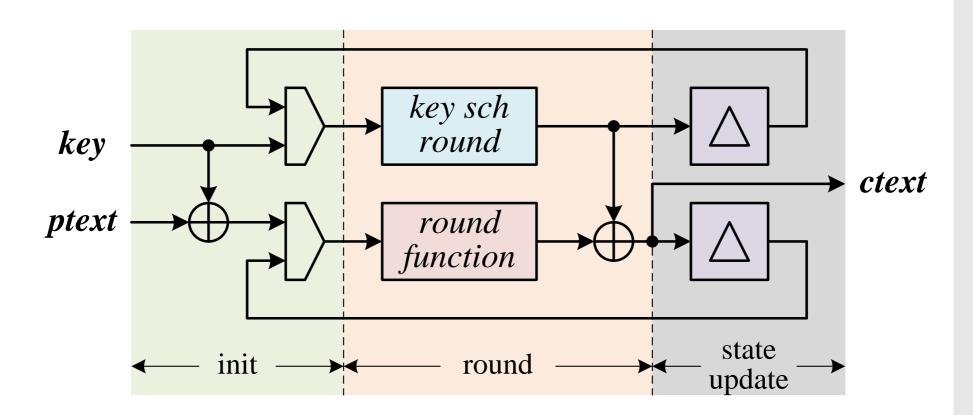


PARALLEL IMPLEMENTATIONS

- Encryption-only
- 128-bit block size:
 - Clefia-128
- 64-bit block size:
 - PRESENT-80
 - mCrypton-96
 - KLEIN-64
 - LED-128
 - PRINCE-128



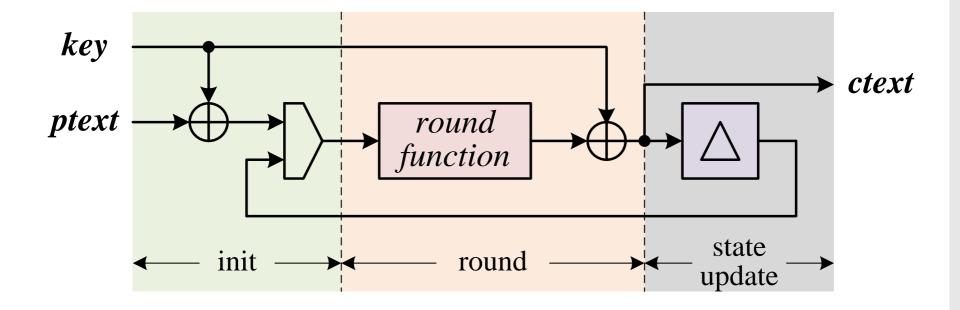
PARALLEL IMPLEMENTATIONS



- Repeated as many rounds as the cipher is defined for
- In the case of PRINCE, final whitening key added to output node



PARALLEL IMPLEMENTATIONS - NO KEY UPDATE



 In some cases there is fixed key or a simple function of the key (LED and PRINCE)

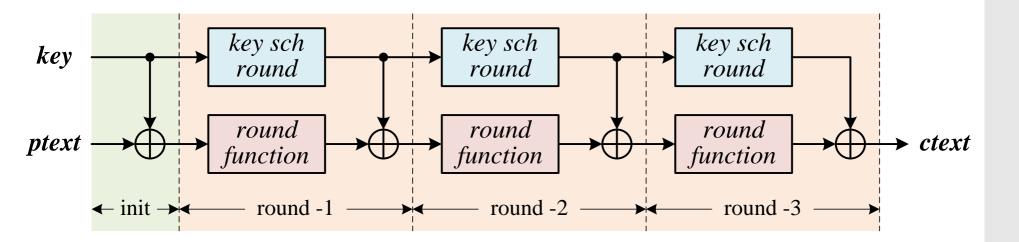


UNFOLDED IMPLEMENTATIONS

- Encryption-only
- 64-bit block size:
 - PRINCE-128



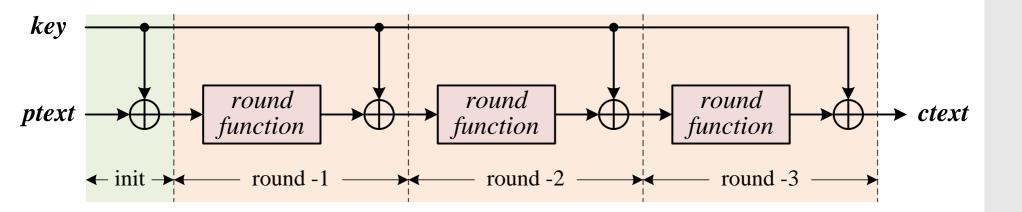
UNFOLDED IMPLEMENTATIONS



Various numbers of round function – as many rounds as the cipher



Unfolded Implementations - No Key Update



- We use this one...
- 12 consecutive round functions for PRINCE



AES IMPLEMENTATIONS

Serial:

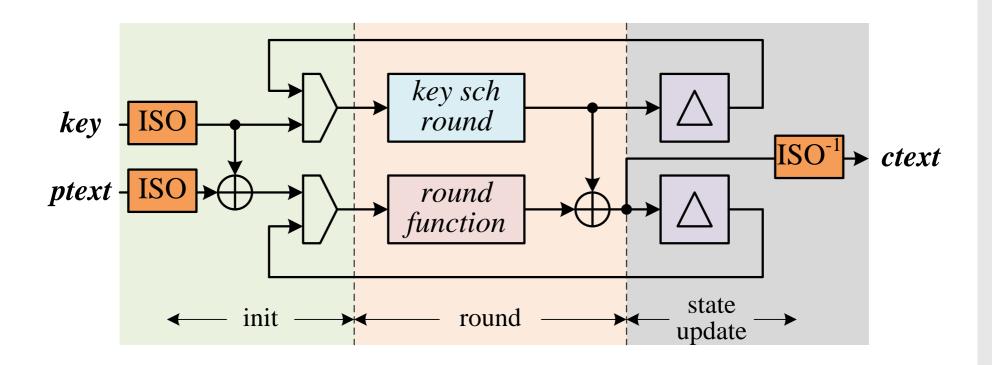
- Byte-based implementation of Moradi et al.
- Uses one S-box implemented in composite field $GF(((2^2)^2)^2)$
- No use of scan flip-flops as suggested: Due to conventional tool flow

Parallel:

- S-box implemented in composite field GF(((2²)⁴)
- S-box implemented in composite field GF(((2²)²)²)
- S-box implemented in composite field $GF(((2^2)^4))$ with isomorphic transform
- S-box implemented in composite field $GF(((2^2)^2)^2)$ with isomorphic transform
- S-box implemented as lookup table



AES IMPLEMENTATIONS — WITH ISOMORPHIC TRANSFORM





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ARCHITECTURAL DECISIONS

- All I/O of ciphers buffered through a flip-flop
- Encryption-only architectures
 - Most modes of operation do not need encryption



EVALUATION OF DESIGN PARAMETERS — TOOLS

- Implementations synthesized in UMC 130 nm low-leakage
 Faraday technology library
- Using Cadence Encounter RTL Compiler
- Simulation tool: Modelsim



EVALUATION OF DESIGN PARAMETERS — METRICS

- Area (GE): Gate Equivalence
 - Dividing silicon area of cipher with a given std-cell library by area of 2-input NAND gate
- Dynamic power: Power when circuit active
 - Proportional to operation frequency
- Static power: Power during no activity
 - Significant for low frequency operation
- Energy/bit:
 - (Total power × Cycle count) / (Frequency × Block length)



EVALUATION OF DESIGN PARAMETERS

- Each module first synthesized for best power
- Generated netlists used to simulate actual module with 100 random keys together with 10 random plaintexts per key to get best statistics
- SAIF files generated in these simulations
- SAIF files sent back to synthesis tool together with netlist to run power analysis



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Results and Discussion

Cipher Architecture	Block	Encryption	Freq.	Area	Static	Dynamic	Energy	Energy
	length	time			Power	Power	per bit	
		(# cycles)	(KHz)	(GEs)	(µW)	(μW)	(pJ/bit)	(nJ)
AES_small_core_1 [12]	128	211	100	3685	6.25	11.31	186.44	37.05
AES_2_2_enc_128	128	10	100	12405	24.46	210.15	164.18	23.46
AES_4_2_enc_128	128	10	100	11453	21.37	135.26	105.67	15.66
AES_iso_2_2_enc_128	128	10	100	15442	30.41	52.85	41.29	8.33
AES_iso_4_2_enc_128	128	10	100	13052	25.19	37.06	28.95	6.23
AES_lut_enc_128	128	10	100	19591	30.81	96.11	75.09	12.69



Results and Discussion

Cipher Architecture	Block/Key	Encryption	Freq.	Area	Static	Dynamic	Energy	Energy
	length	time			Power	Power	per bit	
		(# cycles)	(KHz)	(GEs)	(µW)	(µW)	(pJ/bit)	(nJ)
CLEFIA	128/128	18	100	6941	13.24	37.09	52.19	9.06
KLEIN_parallel	64/64	12	100	2760	4.88	2.18	4.09	0.85
KLEIN_serial	64/64	98	100	1432	2.56	1.48	22.66	3.96
LED	64/128	48	100	3194	5.62	2.34	17.55	3.82
mCrypton	64/96	13	100	3197	5.80	2.50	5.08	1.08
PRESENT	64/80	31	100	2195	3.75	1.14	5.52	3.82
PRINCE_folded	64/128	12	100	2953	5.75	2.80	5.25	1.03
PRINCE_unfolded	64/128	1	100	39938	16.13	120.20	1.46	1.36
Katan_32	32/80	254	100	801	1.52	0.43	34.13	4.94
Katan_48	48/80	254	100	925	1.71	0.49	25.93	5.60
Katan_64	64/80	254	100	1048	1.94	0.56	22.23	6.34



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Conclusion and Future Directions

- Area, power, energy evaluation of
 - 11 lightweight block cipher architectures
 - 6 different AES architectures
- Discussion of power consumption in relation to area
 - LUT-based AES largest in area, best in dynamic power consumption
 - Others depend on complexity of round function
- Dynamic power consumption plays an important role for high frequency operation
 - Try to estimate dynamic power consumption via measuring toggle activity
- Lightweight applications run at low frequency → Static power consumption is also very important



Thanks for Listening!

Any Questions?

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